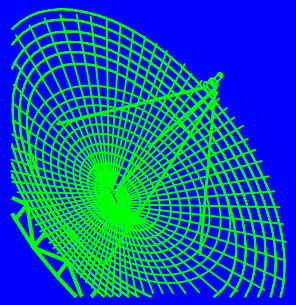
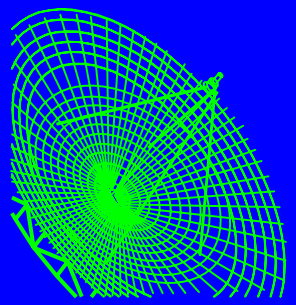


“AstroSoft “ EMC Software

Innovation Simulation Tool for PCB/Package Layout

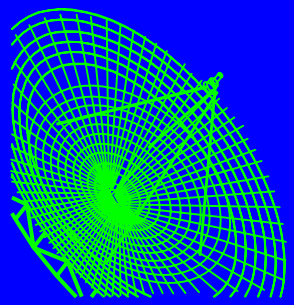
ASTRO Information Technology Inc



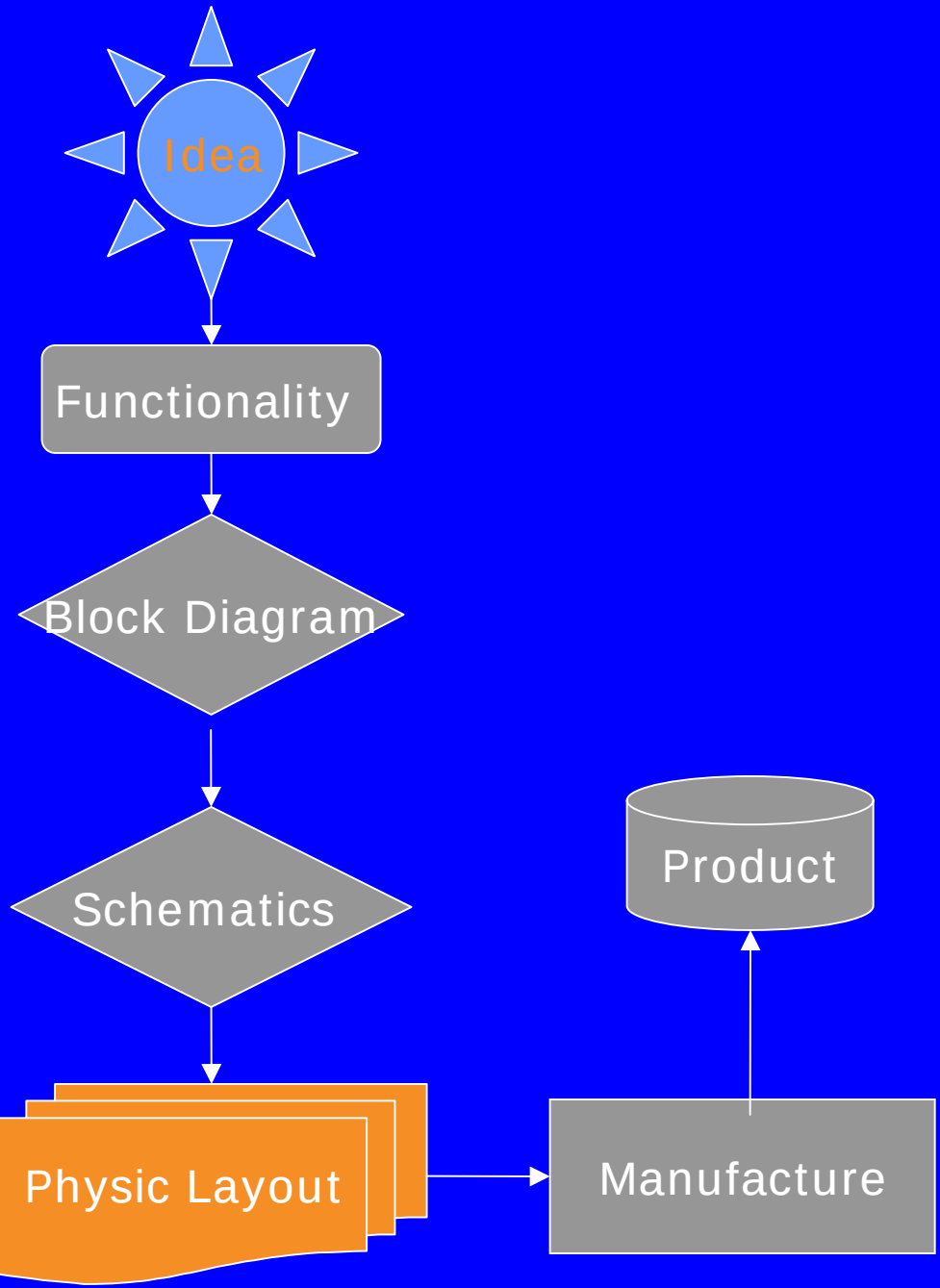
Features of Software

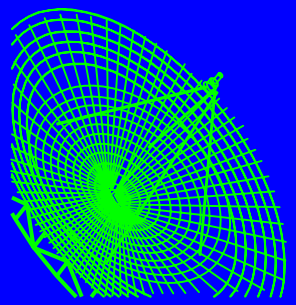
This is a software tool of simulation for PCB/package layout

- Time and frequency domain analysis
- Waveform analysis on each line
- Switching noise on power/ground plane/network analysis
- Cross-talking analysis
- EMC/EMI analysis
- Effect of decoupling
- Voltage/current distribution analysis
- Most devices compatible
- Industry standard data format input
- Text and graphic output



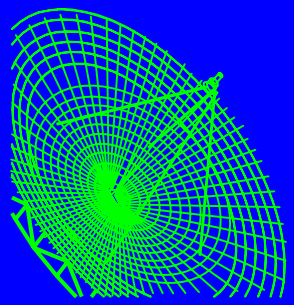
Design Flow


Idea
Functionality
Block Diagram
Schematics
Physic Layout
Manufacture
Product



Issues at Layout

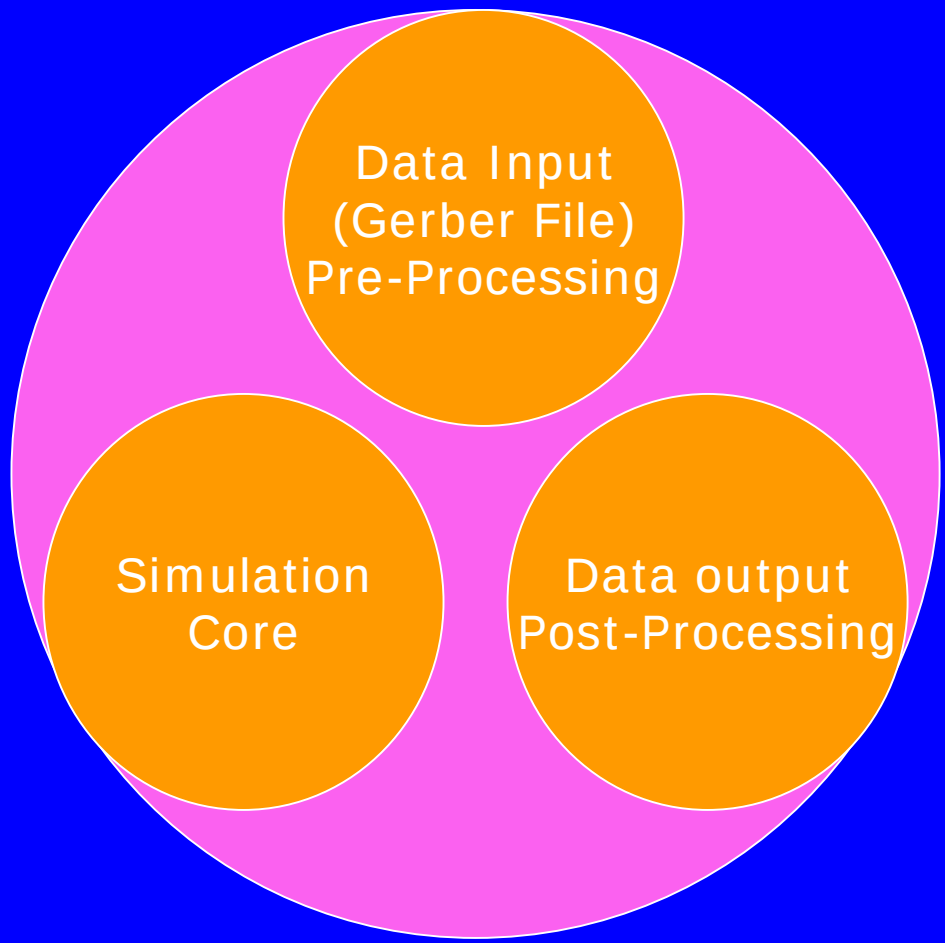
- What is the noise level in each I/O ports?
- How much is the noise in power/ground?
- What signal waveforms look like in each line?
- How much is cross-talking?
- Is any EMC/EMI problem?
- How much via/thu hole effects signal quality?
- Is device placement correct?
- Are the decoupling/bypass capacitors good in both value and location?
- Does the layout work?

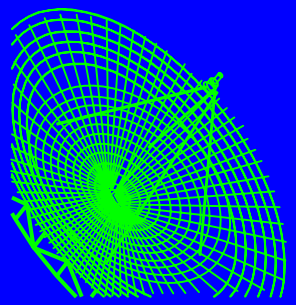


Answer: GTLE Simulator

- Generalized Transmission Line Equation -

GTLE Simulator construction





Data Input and Processing

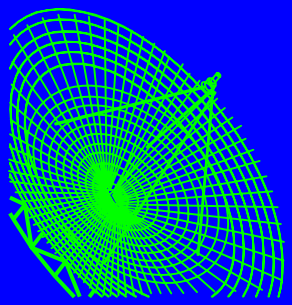
Input data formant: Gerber(RS274X), DXF, …

Parameters extraction:
C, L, R, G for each line and each power/ground plane pair

Parameters extraction:
Power/ground plane geometry re-building

IC's I/O and power/ground setup

Component setup:
- Decoupling/bypass capacitor value and location
- Loads of each line
- EMI ferrite beads value and location

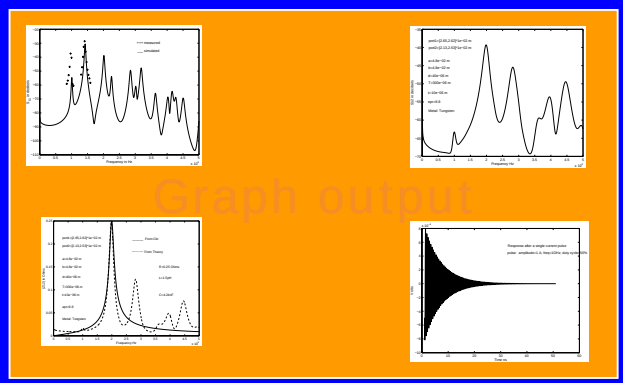


Post-Processing

Data output

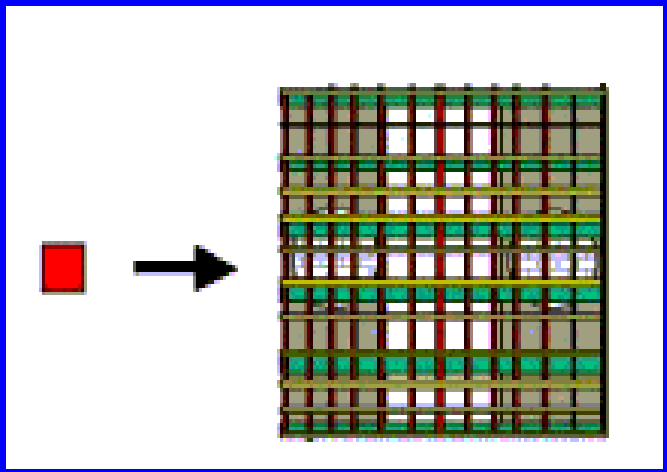
Post Processor

Test File

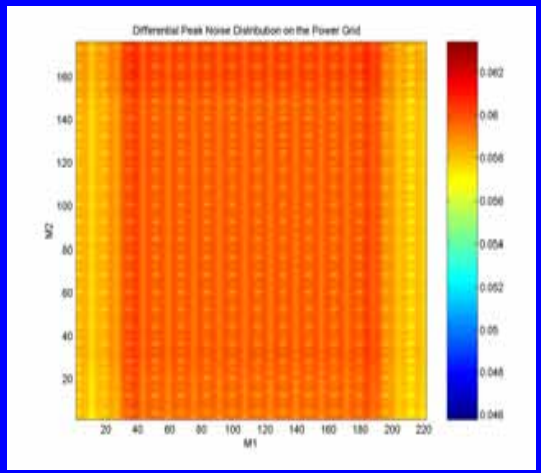


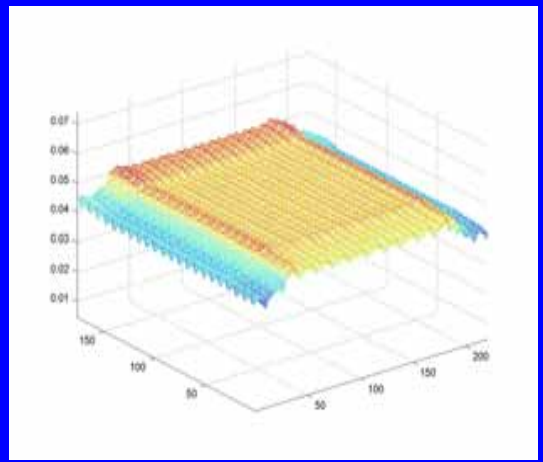
Example I: EMI-Related Noise Simulation On-Chip Power Grid

Chip

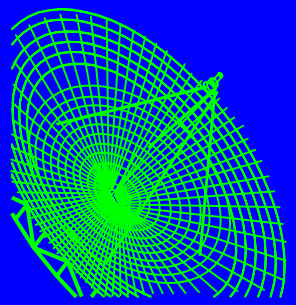


Power/Ground Grid



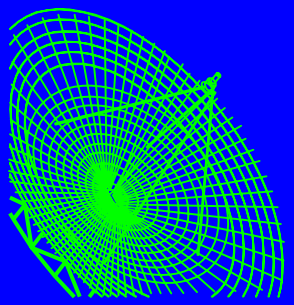


Peak Noise Distribution

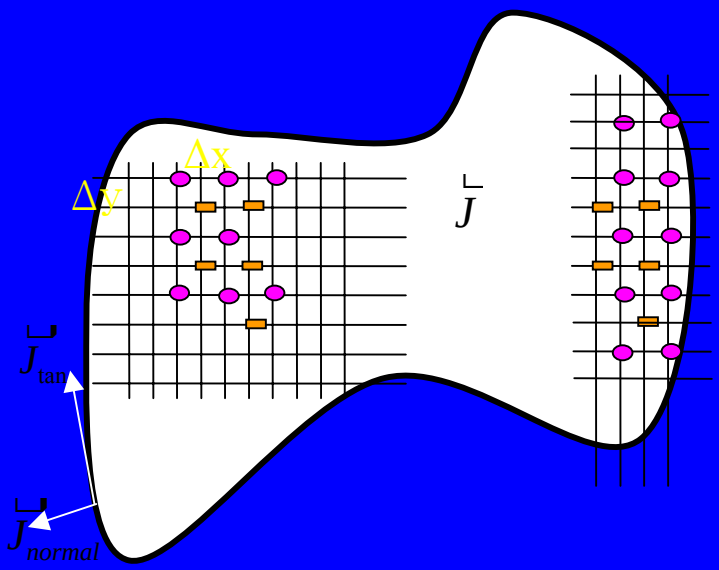


Simulation Approaches
for SSN, Power Distribution, etc.

- Circuitry
  - SIPCE and SPICE Based
  - Modes Order Reduction
  - Distribution Parameter
- EM Field (Maxwell's Equation)
  - FDTD
  - MoM
  - FEM

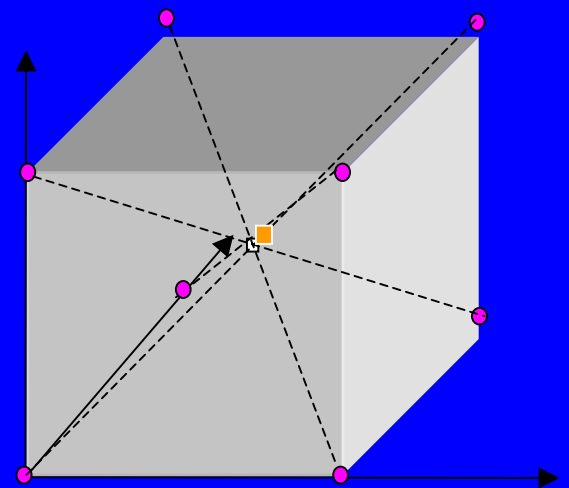


FDTD Technique For Generalized Transmission Line Equations



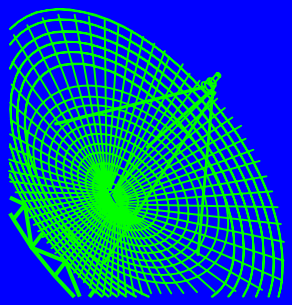
Voltage Current

2-dimension

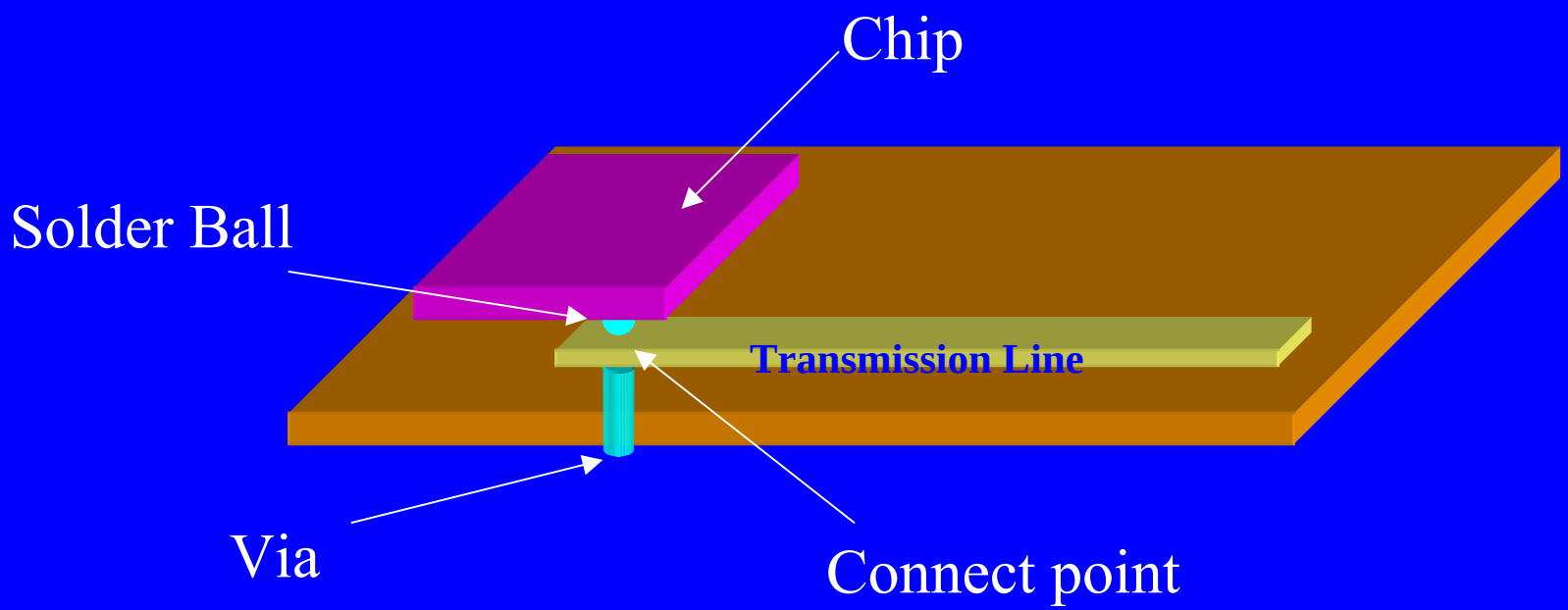


Voltage Current

3-dimension

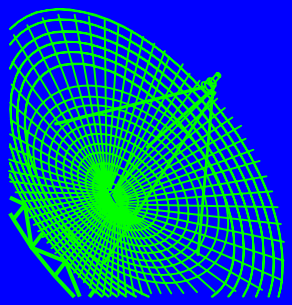


Connection Condition

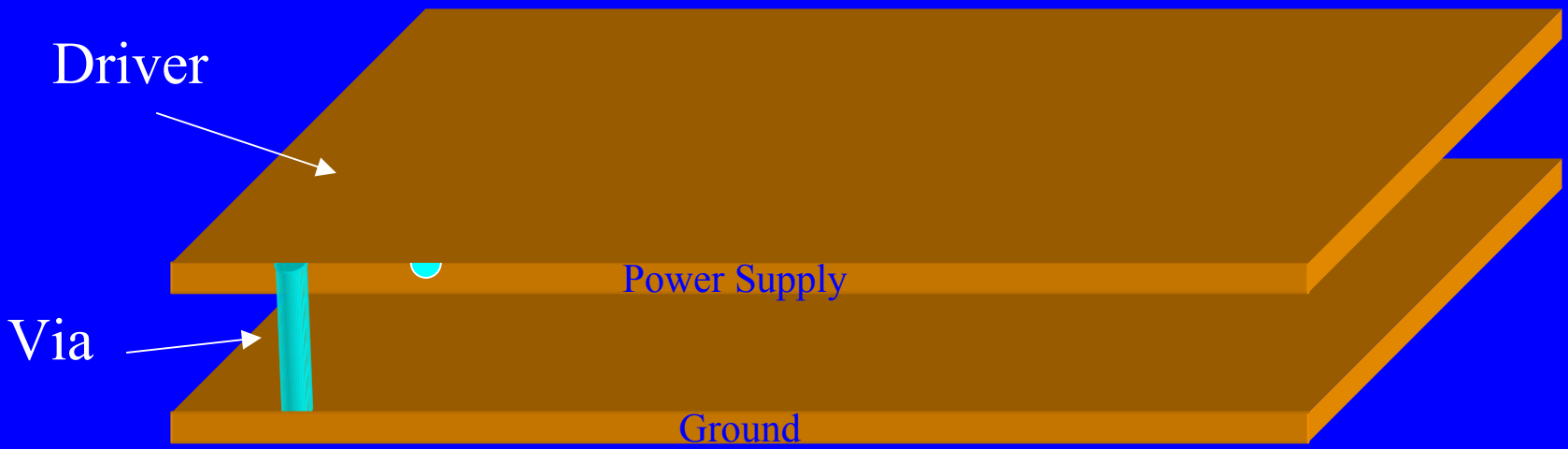


$$V\big|_{solder\ ball} = V\big|_{TL} = V\big|_{Via}$$

At connect point



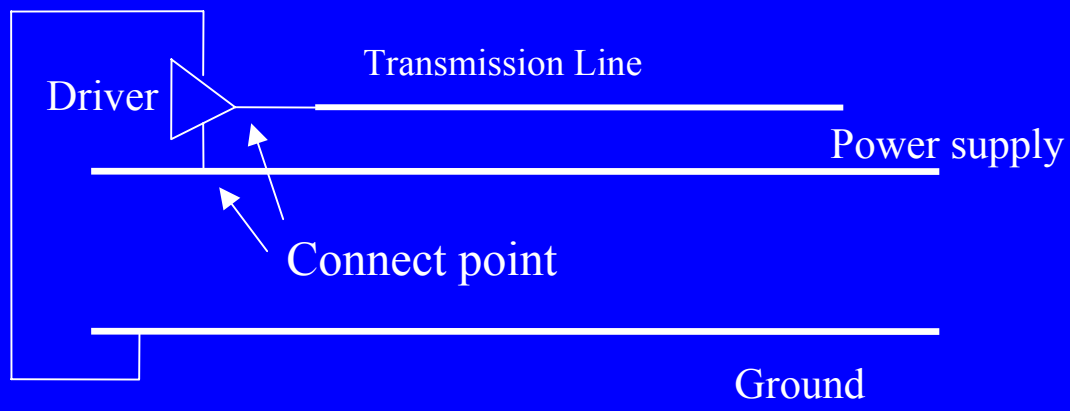
Connection Condition

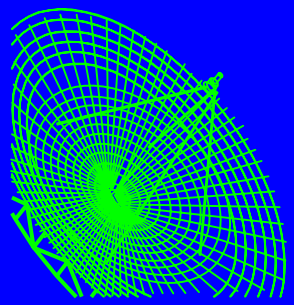


Equivalent circuit

$$V|_{driver} = V|_{power}$$

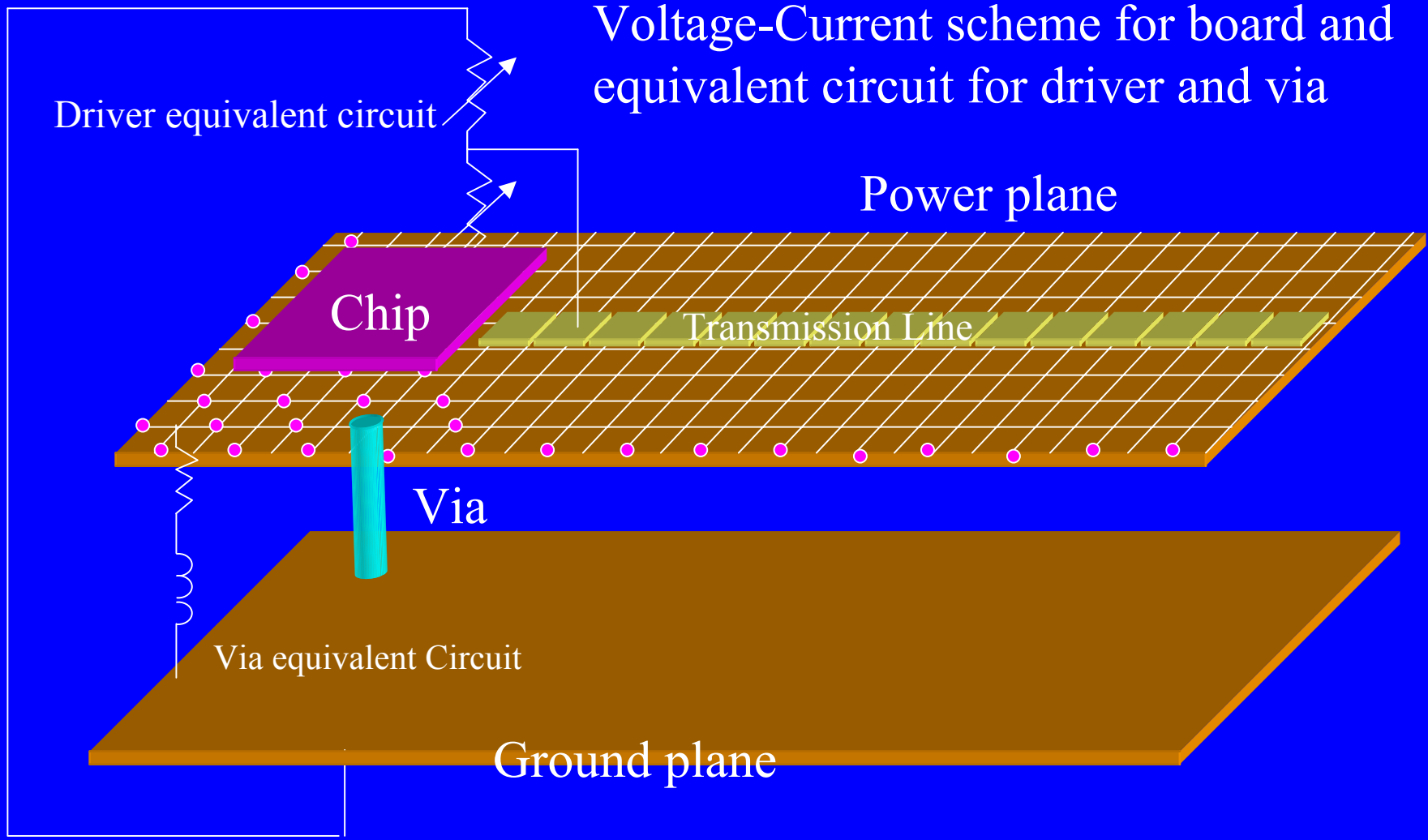
$$V|_{driver\ out} = V|_{TL}$$



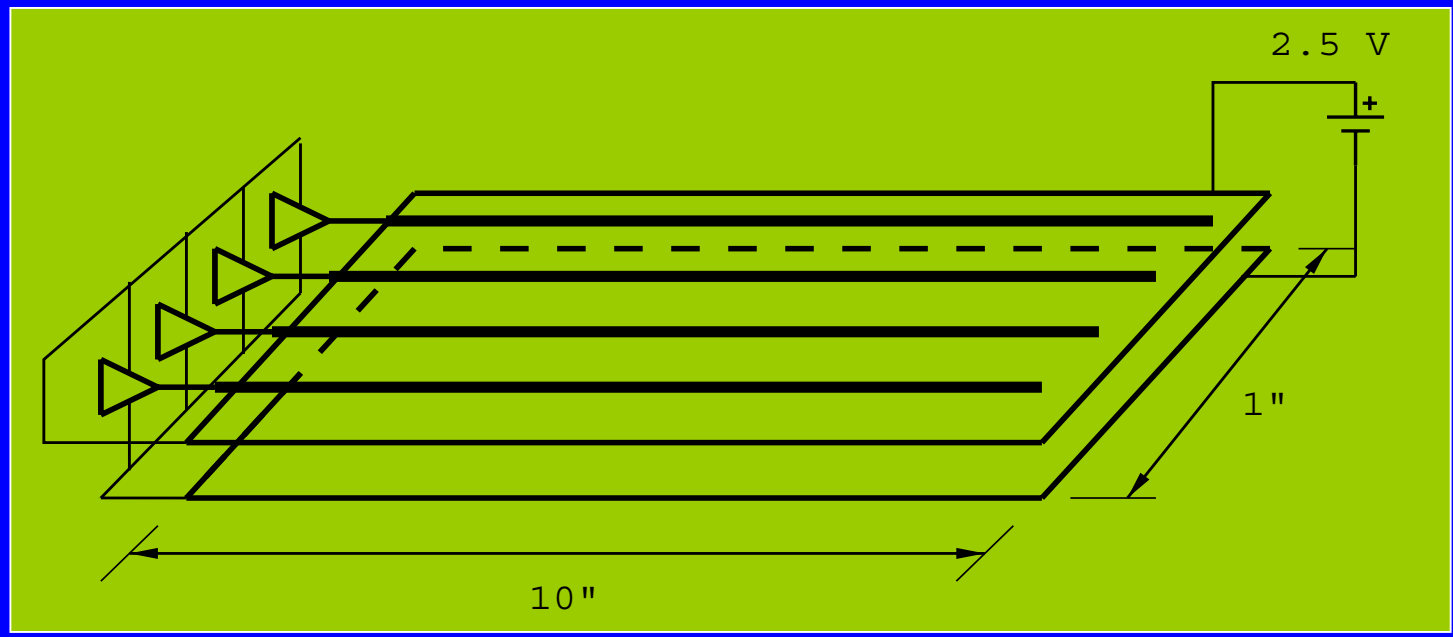


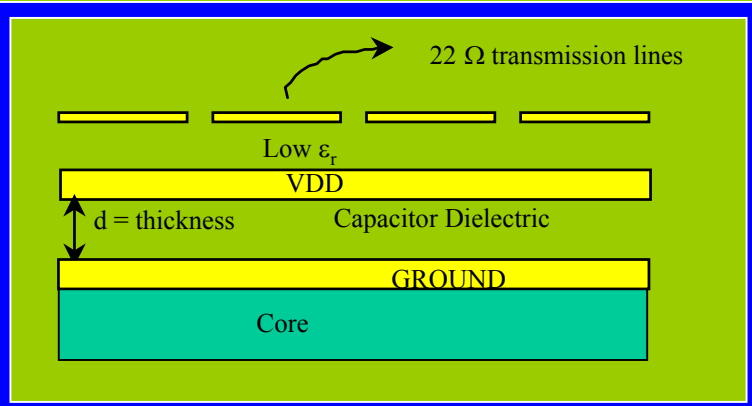
FDTD Technique for GTLE

Voltage-Current scheme for board and equivalent circuit for driver and via

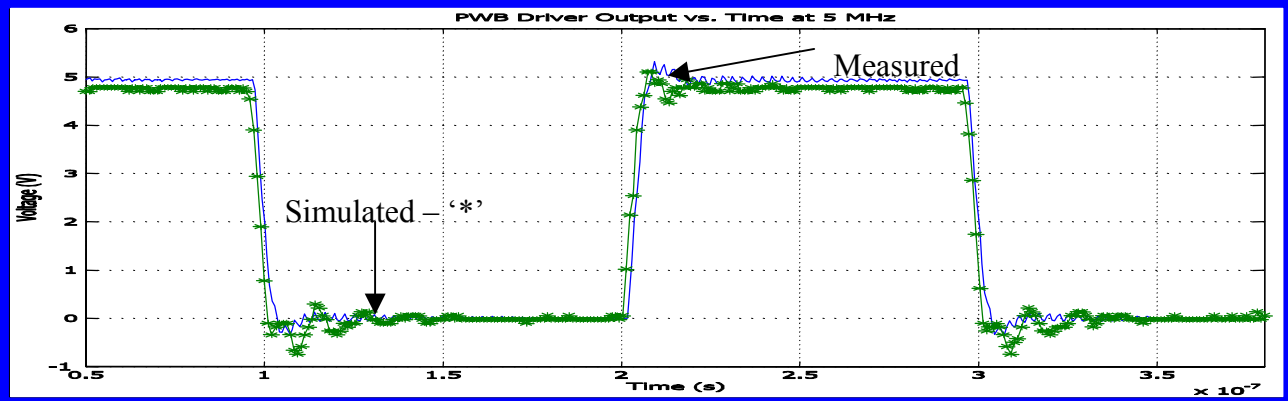


Example II: Test Vehicle for evaluation of SSN Suppression Technique through High ε dielectric material

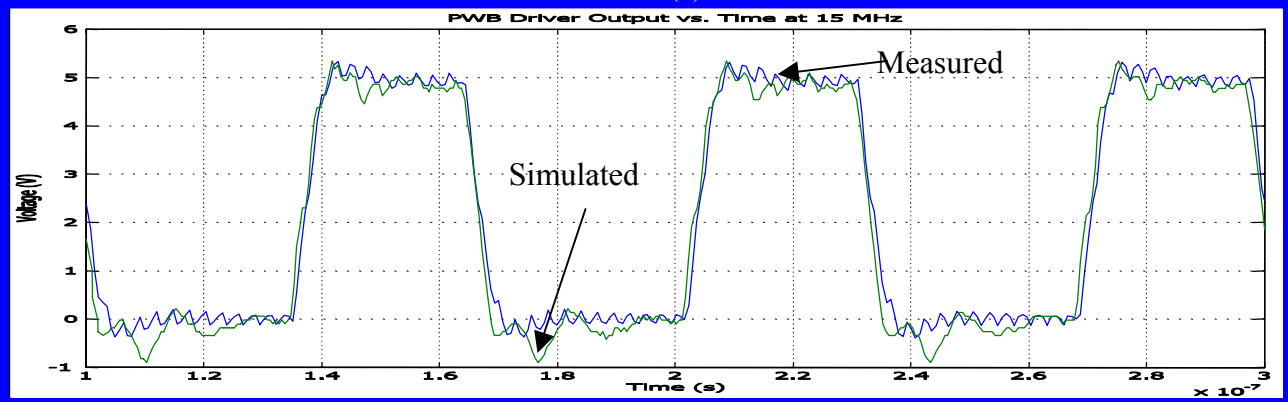




Simulated and measured results



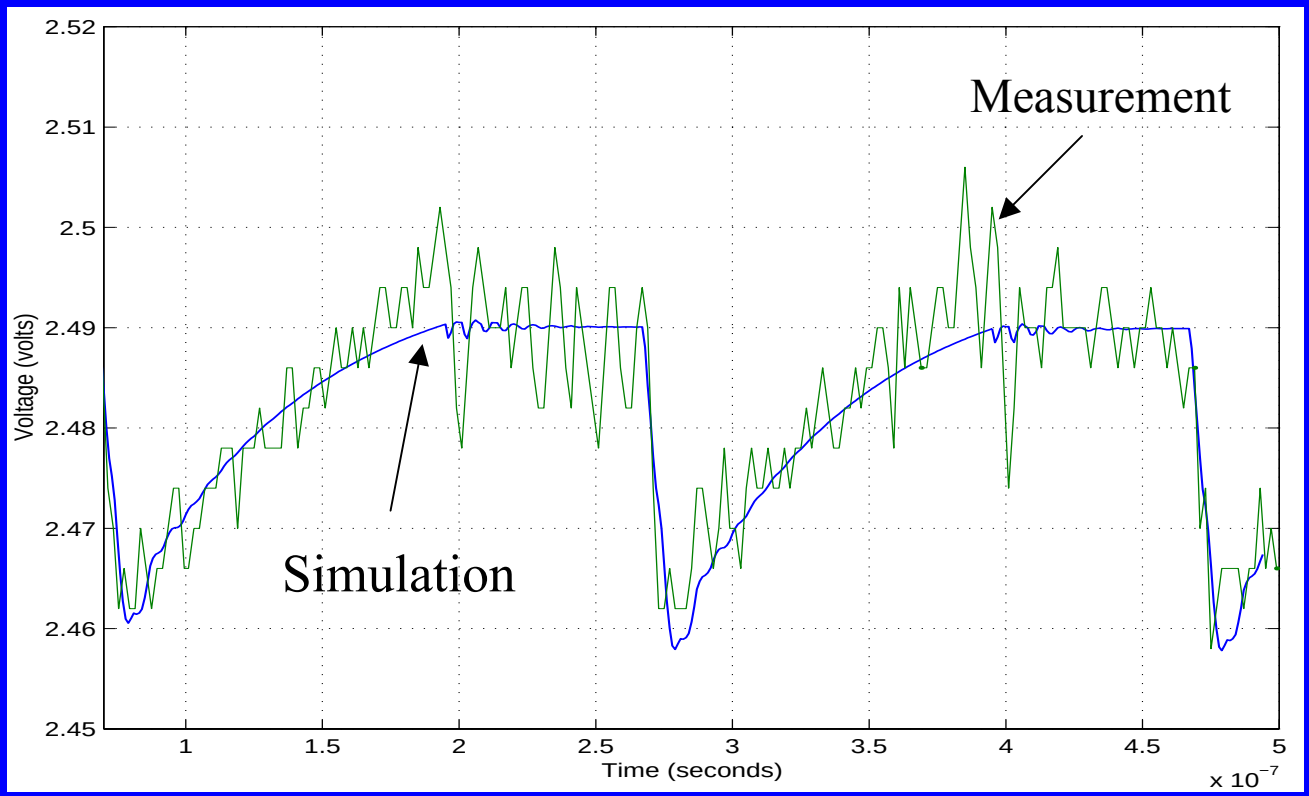
(a)



(b)

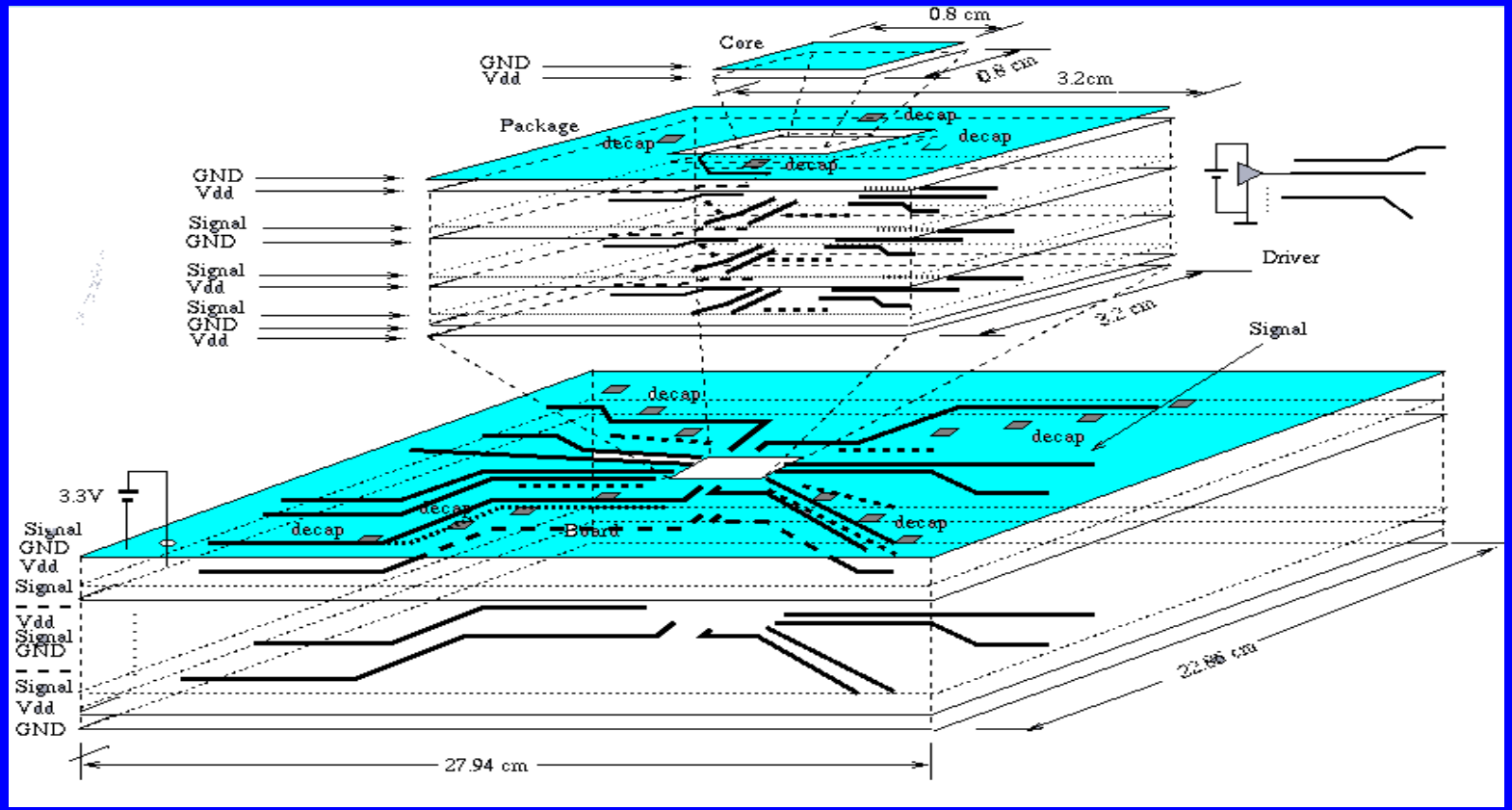
Simulated and Measured Driver Waveform for the Standard PWB without Discrete Decoupling Capacitors at (a) 5 MHz and (b) 15 MHz

Simulated and measured results



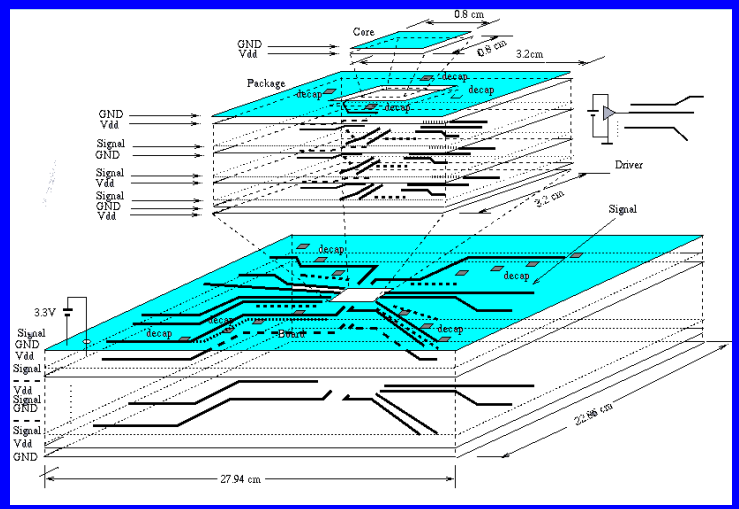
Simulated and measured SSN
without decoupling capacitor at power supply port

Example III: IBM Test Vehicle for Evaluation of SSN and Signal



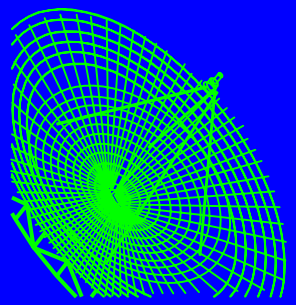
IBM test vehicle 2000

Simulation for evaluation of SSN and signal waveform



Layers: 14(Power/Ground)
6 (signal)
Decoupling Capacitors: 23
Number of Vias: >1000 pairs/plane
Number of Drivers: 144
Number of Traces: 144
Scheme: 100X100/plane
Total cells: 70,000
Number of Time Step: 400,000

Running time: 40 minutes
Storage: 33Mb



Conclusion

Advantage:

- Fast (~ N compare to N^2 of SPICE)
- Small Storage (only on conductor compare to entire region of Maxwell's equation)
- No Matrix Computation
- Add devices, components, Solder Balls Easily without Increasing Running Time
- Arbitrary Geometry

Disadvantage:

- Time Step depends on cell dimension